AMENDMENTS TO CLAIMS:

The listing of claims will replace all prior versions, and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A method for accessing a device by a host using a dedicated bus, the device having up to 2^M memory locations, the bus having N data lines and at least two control lines, wherein M is greater than N, and the host performs an address cycle by asserting a first control signal and a data cycle by de-asserting the first control signal, comprising:

(a) performing a first address cycle to transmit a first address portion over the bus during the first address cycle;

(b) storing the first address portion in a first register of the device in response to detecting the first address cycle;

(c) performing a second address cycle to transmit a second address portion over the bus during the second address cycle;

(d) storing the second address portion in a second register of the device in response to detecting the second address cycle;

(e) performing a first data cycle if the first and second address portions, when combined, form a first address for one of the memory locations;

(f) if the first data cycle is a write data cycle, transmitting a first datum from the host to the device during the first data cycle, and storing the first datum at the first address in response to detecting the first data cycle; and

(g) if the first data cycle is a read data cycle, transmitting a second datum from the device to the host during the first data cycle in response to detecting the first data cycle, the second datum being stored at the first address, wherein the second address cycle is immediately

subsequent to the first address cycle, and the first data cycle is immediately subsequent to the second address cycle.

~~A method for high speed addressing of a memory space having 2^M addresses using an N bit bus, where M is greater than N, comprising the steps of:~~

~~(a) providing at least two registers, each register to store a distinct N bit address byte of a plurality of address bytes that together define an address in the memory space, each register associated with a particular count of address bytes received on the bus;~~

~~(b) receiving a first address byte on the bus;~~

~~(c) producing a first count of address bytes received on the bus as a result of receiving the first address byte;~~

~~(d) selecting a first one of the at least two registers, the first register corresponding with the first count; and~~

~~(e) storing the first address byte in the selected first register.~~

2. (currently amended) The method of claim 1, wherein N equals eight and M equals sixteen. ~~further comprising:~~

~~receiving a second address byte;~~

~~producing a second count of address bytes received on the bus as a result of receiving the second address byte;~~

~~selecting a second one of the at least two registers, the second register corresponding with the second count; and~~

~~storing the second address byte in the selected second register.~~

3. (currently amended) The method of claim 1, further comprising, if the first and second address portions, when combined, are insufficient to form a first address:

(a) performing a third address cycle to transmit a third address portion over the bus during the third address cycle;

(b) storing the third address portion in a third register of the device in response to detecting the third address cycle; and

(e) performing the first data cycle if the first, second, and third address portions, when combined, form a first address for one of the memory locations, wherein the third address cycle is immediately subsequent to the second address cycle, and the first data cycle is immediately subsequent to the third address cycle.

~~2. further comprising the steps of:~~

~~receiving a memory access command; and~~

~~accessing the memory space at an address defined by the first and second address bytes as a result of the memory access command.~~

4. (cancelled)

5. (cancelled)

6. (cancelled)

7. (cancelled)

8. (cancelled)

9. (cancelled)

10. (cancelled)

11. (cancelled)

12. (currently amended) A device ~~An apparatus for high speed addressing of a memory space having 2^M addresses~~, comprising:

~~(a)~~ at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in a ~~the~~ memory space having 2^M addresses, each register associated with a particular count of address-bytes received on a dedicated ~~the~~ bus for coupling the device and a processor, the bus having N data lines and at least two control lines, where M is greater than N;

a memory having a plurality of memory locations; and

~~(b) an N-bit bus, where M is greater than N;~~

~~(c) first and second control signal lines; and~~

a unit to monitor control signals on the bus, the unit including:

~~(d) a logic circuit coupled with the bus, the first and second control signal lines, and the at least two registers, the logic circuit to select one of the at least two registers, the logic circuit including:~~

(a) ~~(i)~~ a K-bit address-byte-received counter to count address-bytes received on the bus by counting each assertion of an address transfer signal on a ~~the~~ first control ~~signal~~ line ~~when a write signal is asserted on the second control signal line~~, wherein the number of the at least two registers is less than or equal to 2^K; ~~; and~~

(b) ~~(ii)~~ a selecting unit to select one of the at least two registers according to a ~~the~~ count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the at least two registers for a particular count value of the address-byte-received counter;

(c) first logic to store an address-byte received on the bus in a currently selected register and to combine address-bytes stored in the at least two registers to form an address for one of the memory locations in response to detecting an assertion of the address transfer signal, and

(d) second logic to store a data-byte received on the bus at the address in response to detecting a de-assertion of the address transfer signal and assertion of a write signal, to fetch a data-byte stored at the address from the memory in response to detecting a de-assertion of the address transfer signal and assertion of a read signal, and to reset the address-byte received counter in response to detecting a de-assertion of the address transfer signal and assertion of one of the write or read signals.

13. (currently amended) The apparatus of claim 12, wherein N equals eight and M equals sixteen. ~~the logic circuit stores a received address byte in a selected one of the at least two registers.~~

14. (cancelled)

15. (cancelled)

16. (cancelled)

17. (cancelled)

18. (cancelled)

19. (cancelled)

20. (cancelled)

21. (cancelled)

22. (cancelled)

23. (currently amended) A machine readable medium embodying a program of instructions for execution by a machine to perform a method for accessing a device by a host using a dedicated bus, the device having up to 2^M memory locations, the bus having N data lines and at least two control lines, wherein M is greater than N, and the host performs an address cycle by asserting a first control signal and a data cycle by de-asserting the first control signal, comprising:

(a) performing a first address cycle to transmit a first address portion over the bus during the first address cycle;

(b) storing the first address portion in a first register of the device in response to detecting the first address cycle;

(c) performing a second address cycle to transmit a second address portion over the bus during the second address cycle;

(d) storing the second address portion in a second register of the device in response to detecting the second address cycle;

(e) performing a first data cycle if the first and second address portions, when combined, form a first address for one of the memory locations;

(f) if the first data cycle is a write data cycle, transmitting a first datum from the host to the device during the first data cycle, and storing the first datum at the first address in response to detecting the first data cycle; and

(g) if the first data cycle is a read data cycle, transmitting a second datum from the device to the host during the first data cycle in response to detecting the first data cycle, the second datum being stored at the first address, wherein the

second address cycle is immediately subsequent to the first address cycle, and the first data cycle is immediately subsequent to the second address cycle.

~~for high-speed addressing of a memory space having 2^M addresses using an N-bit bus, the machine having at least two registers, each register to store a distinct N-bit address byte of a plurality of address bytes that together define an address in the memory space, each register associated with a particular count of address bytes received on the bus, where M is greater than N, comprising the steps of:~~

~~(a) receiving a first address byte on the bus;~~

~~(b) producing a first count of address bytes received on the bus as a result of receiving the first address byte;~~

~~(c) selecting a first one of the at least two registers, the first register corresponding with the first count; and~~

~~(d) storing the first address byte byte in the selected first register.~~

24. (currently amended) The machine readable medium of claim 23, wherein N equals eight and M equals sixteen. ~~the method further comprising the steps of:~~

~~receiving a second address byte;~~

~~producing a second count of address bytes received on the bus as a result of receiving the second address byte;~~

~~selecting a second one of the at least two registers, the second register corresponding with the second count; and~~

~~storing the second address byte in the selected second register.~~

25. (currently amended) The machine readable medium of claim 23, further comprising, if the first and second address portions, when combined, are insufficient to form a first address:

(a) performing a third address cycle to transmit a third address portion over the bus during the third address cycle;

(b) storing the third address portion in a third register of the device in response to detecting the third address cycle; and

(e) performing the first data cycle if the first, second, and third address portions, when combined, form a first address for one of the memory locations,

wherein the third address cycle is immediately subsequent to the second address cycle, and the first data cycle is immediately subsequent to the third address cycle.

~~24. the method further comprising the steps of:~~

~~receiving a memory access command; and~~

~~accessing a memory at an address defined by the first and second address bytes as a result of the memory access command.~~

26. (cancelled)

27. (cancelled)

28. (cancelled)

29. (cancelled)

30. (cancelled)

31. (cancelled)

32. (cancelled)

33. (cancelled)

34. (cancelled)

35. (cancelled)

36. (cancelled)

37. (currently amended) A system, comprising:

~~(a) an N-bit bus, where M is greater than N;~~

~~(b) a memory having 2^M addresses;~~

~~(c)~~ a central processing unit, ~~coupled with the bus, to transmit at least two address bytes that together define an address in a the memory space having 2^M addresses, wherein M is greater than N, and to transmit a memory access command;~~;

a device having:

~~(d)~~ at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in a ~~the~~ memory space having 2^M addresses~~, each register associated with a particular count of address-bytes received on the bus~~;

a memory having a plurality of memory locations;

~~(e) first and second control signal lines;~~

a unit to monitor control signals on the bus, the unit including:

~~(f) a logic circuit coupled with the bus, the first and second control signal lines, and the at least two registers, the logic circuit to receive and store address-bytes in a selected one of the at least two registers, the logic circuit including:~~

(a) ~~(i)~~ a K-bit address-byte-received counter to count address-bytes received on a ~~the~~ bus by counting each assertion of an address transfer signal on a ~~the~~ first control ~~signal~~ line ~~when a write signal is asserted on the second control signal line~~, wherein the number of the at least two registers is less than or equal to 2^K~~;~~ ~~and~~

(b) ~~(ii)~~ a selecting unit to select one of the at least two registers according to a ~~the~~ count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the at least two registers for a particular count value of the address-byte-received counter~~;~~ ~~and~~

~~(g) a unit to:~~

~~(i) receive the memory access command; and~~

~~(ii) access the memory at an address defined by the first and second address-bytes as a result of the memory access command.~~

(c) first logic to store an address-byte received on the bus in a currently selected register and to combine address-bytes stored in the at least two registers to form an address for one of the memory locations in response to detecting an assertion of the address transfer signal, and

(d) second logic to store a data-byte received on the bus at the address in response to detecting a de-assertion of the address transfer signal and assertion of a write signal, to fetch a data-byte stored at the address from the memory in response to detecting a de-assertion of the address transfer signal and assertion of a read signal, and to reset the address-byte received counter in response to

detecting a de-assertion of the address transfer signal and assertion of one of the write or read signals; and

the bus to exclusively couple the central processing unit and the device, the bus having N data lines and at least two control lines, where M is greater than N.

38. (currently amended) The system of claim 37, wherein N equals eight and M equals sixteen. ~~the memory access command is a write command.~~

39. (cancelled)

40. (cancelled)

41. (cancelled)

42. (cancelled)

43. (cancelled)

44. (cancelled)

45. (cancelled)

46. (cancelled)

47. (cancelled)

48. (cancelled)

49. (cancelled)

50. (cancelled)